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COMBINATION TRIANGULAR WAVEFORM GENERATOR AND TRIANGULAR TO PSEUDO-SINUSOIDAL WAVEFORM CONVERTER CIRCUIT

Cross Reference to Related Application

[0001] This application claims priority of U.S. Provisional Patent Application No. 60/409,893 filed on September 10, 2002 entitled "Combination Triangular Waveform Generator and Triangular to Pseudo-Sinusoidal Waveform Converter Circuit" and the teachings thereof are incorporated herein by reference.

Background of the Invention

[0002] Waveform generators are widely used in switching power supply devices, function generators, filter tuning circuitry and motor driving devices.

[0003] A conventional sinusoidal waveform generator generally comprises two stages. The first stage is a triangle waveform generator and the second stage is a converter which converts the triangular waveform to a sinusoidal waveform. The triangular waveform generator generally comprises a current source, a polarity switch and a means of capacitance, such as one or a plurality of capacitors. The triangular-to-sinusoidal converter generally comprises several diodes and resistors. The triangular-to-sinusoidal converter takes advantage of a diode's nonlinear function to rectify and shape the waveform.

[0004] Disadvantageously, the nonlinear functions of the diodes in the conventional triangular-to-sinusoidal converter typically require as many current paths as there are diodes. As a result, the triangular-to-sinusoidal converter has high power consumption. Further, the number of diodes and resistors in the triangular-to-sinusoidal converter affects the surface area of the converter. In addition, an integrator, which requires a device with

large capacitance, also affects the surface area. Not surprisingly, then, the surface area is typically large in comparison to the surface area taken by other elements in a circuit.

[0005] More specifically, the conventional triangular-to-sinusoidal converter comprises several sub-stage elements. The first sub-stage element comprises an up-down counter with an input and output. A continuous triangular wave is fed into the up-down counter input and converted into a digital triangular wave which is made available on its output. A second sub-stage element is coupled to the output of the first sub-stage element. The second sub-stage element is a read only memory ("ROM"), also having an input and an output. The digital triangular waveform is taken from the output of the first sub-stage element and is fed into the input of the ROM. The digital triangular wave is converted into a digital sinusoidal waveform and made available on the output of the ROM. A third sub-stage element coupled to the output of the second sub-stage element is a digital-to-analog converter. The third sub-stage element accepts the digital sinusoidal waveform and converts it to a continuous analog sinusoidal waveform at the output. The fourth sub-stage element is a post analog filter with an input and an output. It accepts the continuous sinusoidal waveform on the input and outputs a smoother sinusoidal signal. As noted, the

sinusoidal waveform generator disadvantageously requires a large surface area for the placement of its constituent components. The high power consumption of the triangular-to-sinusoidal waveform generator is attributable to the requirements of the up-down counter, read only memory, digital to analog converter and post analog filter.

Summary of the Invention

[0006] Because of the surface area and power consumption disadvantages of the conventional triangular-to-sinusoidal waveform converter circuit, a small, fairly non-complex triangular waveform generator and pseudo-sinusoidal waveform converter circuit is desired. The present invention comprises a triangular voltage waveform generator and triangular to pseudo-sinusoidal current waveform converter. The outputs of the present invention are preferably differential, although the invention can easily be modified for single ended output. The frequency of the output waveforms corresponds to the frequency of the input reference clock.

[0007] The present invention can be viewed as being comprised of three sub-circuits. The first sub-circuit is a triangular waveform generator for the generation of two triangular waveforms. The second sub-circuit is an amplitude control circuitry that controls the amplitude of triangular waveform needed to generate a pseudo-sinusoidal waveform. The third sub-circuit is a reference voltage circuit which controls the amplitude control circuitry. This third sub-circuit is operable to generate reference voltages for the peak

voltages of the triangular waveform.

[0008] The present invention advantageously utilizes one circuit to generate two kinds of waveforms. The triangular waveform voltage is generated from an external digital clock and its current is controlled by the circuitry of the present invention. Further, the common voltage of the triangular waveforms is self-controlled by the circuit using feedback.

[0009] This circuit topology can also be utilized as a differential current mirror. The pseudo-sinusoidal waveform current is converted from a triangular waveform by the triangular waveform converter to a pseudo sinusoidal waveform in the circuit.

Brief Description of the Drawings

[0010] Figure 1 is an overall block diagram of triangular waveform generator and the triangular to pseudo-sinusoidal waveform converter of the present invention;

[0011] Figure 2 is a circuit diagram of the sinusoidal waveform and triangular waveform generator;

[0012] Figure 3 is a circuit diagram of the reference voltage generator;

[0013] Figure 4 is a circuit diagram of a voltage to current converter utilizing a NOT gate switch;

[0014] Figure 5 is a circuit diagram of a voltage to current converter;

[0015] Figure 6 is a circuit diagram of a current comparator and current generator as seen in Figure 1; and

[0016] Figure 7 is a timing diagram of the present invention.

Detailed Description of the Present Invention

[0017] The present invention comprises two waveform generators, a reference voltage generator and amplitude control circuitry. Generally, a separate reference clock signal is applied to the input of each of the two waveform generators, there being a 90 degree phase difference between the two clock signals. Further, reference currents are supplied to the two waveform generators from the amplitude control circuitry. The waveform generators combine the reference currents and the clock signals into two triangular waveforms with 90 degrees phase difference. The reference currents determine the amplitude of the triangular waveform.

[0018] Two reference voltages, one for high side, the other for the low side, are generated in the reference voltage circuitry. The two reference voltages are supplied to the amplitude control circuitry which generates the reference currents to compare to the triangular waveform amplitude. The amplitude control circuitry also rectifies the triangular waveform and derives the amplitude of the triangular waveform. It continuously compares the reference voltage to the amplitude of the triangular waveform to control the supply of the reference currents for the waveform generator. The amplitude control circuitry is

operable to ensure that the amplitude of the triangular waveform remains constant.

[0019] The second sub-circuit comprises the voltage-to-current converter, rectifier and current comparator. As noted, two triangular waveforms are generated by the triangular waveform generators. These two triangular waveforms have 90 degree of phase offset from each other and have same amplitude. The waveform voltages and reference voltages are converted into current signals by the voltage to current converter. The value of the triangular waveform amplitude is added to the absolute value of each triangular waveforms in the rectifier. This derived amplitude is compared to the converted current from the reference voltages. The comparator, which has limited gain, directly controls the reference current of the waveform generator. The advantage of this method is that the amplitude of the triangular waveform can be compared to the reference voltage continuously. This method results in high rectifier efficiency.

[0020] The conventional method of generating a pseudo-sinusoidal waveform compares both peaks of the triangular waveform to the reference voltage for a moment. As such, the conventional method requires an integrator at the compared output due to the need of the comparator to compare the amplitude of the triangular waveform to the reference voltage in

discrete time. Because the comparator has limited speed, the short time comparison causes a frequency dependence of the amplitude.

[0021] The third sub-circuit of the present invention comprises the sinusoidal waveform converter. A maximum peak to peak voltage of the triangular waveform has to be an appropriate input voltage for the sinusoidal waveform converter. The appropriate input voltage for the sinusoidal waveform converter is defined as the maximum voltage that will not saturate the output current of the sinusoidal waveform converter. Consequently, the level of current that will not saturate the output current of the sinusoidal waveform is the maximum output current.

[0022] In operation, target differential currents are input into the output nodes of the sinusoidal waveform converter. The objective appropriate input voltage is the balance of the target output current with input current provided by a feed-back connection. The foregoing operation of the present invention is more specifically described in the following detailed descriptions of the drawings.

[0023] As seen in Figure 1, clock signal A 102 and clock signal B 103 are input to the core of the waveform generators 170 and 180. These clock signals have 90 degrees phase

difference as seen in Figure 7A and Figure 7B. Reference currents 104 and 105 are input to the core of the waveform generators 170 and 180. The core of the waveform generators 170 and 180 generate triangular waveforms 140, 150 and sinusoidal waveforms 130 and 131 as also seen in Figure 7H, from input currents 104 and 105 and clock signal 102 and clock signal 103. These triangular waveforms, as also seen in Figure 7C and Figure 7D have same amplitude and 90 degrees phase difference. The triangular waveforms 140 and 150 are provided to the inputs of the voltage-to-current converters 106 and 107. In addition, reference voltage 160 is generated in the reference voltage generator 110. The reference voltages 160 are input to the voltage-to-current generator 110. Currents from the voltage-to-current generator 110 and from the core of the waveform generators 170 and 180 are input to switches inside of the voltage to current converters 106 and 107. The respective switches are driven by the other side's clock signal 103 and 102. This configuration controls the absolute value of the output, as seen in Figures 7E and 7F. Output currents from voltage-to-current generators 106, 107 and 110 are summed at node 108, as seen in Figure 7G and are provided to the input of the current comparator and current bias generator 120. The current comparator therein compares the input differential currents at input 109. If the current is less than 0, a current bias generator within current comparator

and current bias generator 120 increases the reference currents 104 and 105. As such, the amplitude of triangular waveform will be increased.

[0024] The equations governing rectifier operation is as follows:

Triangular waveform(tri) phase=0

$$tri(\phi) = \frac{\phi}{\pi} + \frac{1}{2} \qquad @ \qquad -\pi \le \phi < 0$$

$$tri(\phi) = -\frac{\phi}{\pi} + \frac{1}{2} \qquad @ \qquad 0 \le \phi < \pi$$

Triangular waveform (tri) phase=$\frac{\pi}{2}$

$$tri(\phi + \frac{\pi}{2}) = -\frac{\phi}{\pi} - 1 \qquad @ \qquad -\pi \le \phi < -\frac{\pi}{2}$$

$$tri(\phi + \frac{\pi}{2}) = \frac{\phi}{\pi} \qquad @ \qquad -\frac{\pi}{2} \le \phi < \frac{\pi}{2}$$

$$tri(\phi + \frac{\pi}{2}) = -\frac{\phi}{\pi} + 1 \qquad @ \qquad \frac{\pi}{2} \le \phi < \pi$$

This calculation results in the following:

$$|tri(\phi)| + |tri(\phi + \frac{\pi}{2})| = -(\frac{\phi}{\pi} + \frac{1}{2}) - (-\frac{\phi}{\pi} - 1) = \frac{1}{2} \qquad @ \qquad -\pi \le \phi < -\frac{\pi}{2}$$

$$|tri(\phi)| + |tri(\phi + \frac{\pi}{2})| = (\frac{\phi}{\pi} + \frac{1}{2}) - (\frac{\phi}{\pi}) = \frac{1}{2} \qquad @ \qquad -\frac{\pi}{2} \le \phi < 0$$

$$|tri(\phi)| + |tri(\phi + \frac{\pi}{2})| = (-\frac{\phi}{\pi} + \frac{1}{2}) + (\frac{\phi}{\pi}) = \frac{1}{2} \qquad @ \qquad 0 \le \phi < \frac{\pi}{2}$$

$$|tri(\phi)| + |tri(\phi + \frac{\pi}{2})| = -(-\frac{\phi}{\pi} + \frac{1}{2}) + (-\frac{\phi}{\pi} + 1) = \frac{1}{2} \qquad @ \qquad \frac{\pi}{2} \le \phi < \pi$$

[0025] The bias voltage is generated in the current bias generator of current comparator

and current bias generator 120.

[0026] The circuitry of waveform generator 170 is shown in Figure 2. As seen in Figure 2, the terms top and tom refer to the nodes for the triangular waveform differential voltage outputs. The terms sop and som refer to the nodes for the sinusoidal differential current waveform outputs. As seen in Figure 2, the current to charge the capacitor 201 is generated with transistor 210 from the bias voltage. The capacitor 201 is connected as differential. It can be easily modified as single-ended. For example, two capacitors are connected between top and GND and between tom and GND. All transistors used herein are preferably MOSFETs, although other transistor compositions can be used. The current is defined as Ir. A clock signal is provided to the circuit at input pin clk. The clock signal is supplied to the gate of transistor 212 for switching. The inverted clock signal is supplied to gate of transistor 211 for switching. As seen in Figure 2, the sources of transistor 211 and transistor 212 are coupled. In operation, if transistor 211 is on, then transistor 222 is off, because when clk is high, the inverter output is low. Current Ir flows from the source of transistor 211 through the drain of the transistor 211. The source coupled transistor 211 and transistor 212 result in a differential current. It is this differential current

that charges capacitor 201. As a result, voltage at the node top 220 is increased. The drain current of transistor 215 and transistor 216 are equal, because the both gate-source voltages are equal. Transistors 215 and 216 generate common current. In order to increase the voltage of the node top 220, the gate-source voltage of transistor 215 and transistor 216 must increase because the coupled sources of transistor 213 and transistor 214 are connected to the gates of transistor 215 and transistor 216. When the voltage of tom is decreased, the drain current of transistor 216 charges capacitor 201 and the voltage at node tom 222 is decreased. The differential voltage across capacitor 201 thus increases and the drain current of transistor 213 increases. The drain current of transistor 214 decreases as the voltage across capacitor 201 increases. The differential voltage across capacitor 201 is first order linear, because a constant current charges the capacitor 201. The drain current of transistor 213 and transistor 214 is given by the differential transistor pair V-I characteristic, because the differential voltage between the gate of transistor 213 and the gate of transistor 214 increases in a linear first order manner. The current through transistor 213 increases from point A to point B as seen in Figure 7H.

[0027] If transistor 212 is on and transistor 211 is off, the current Ir flows from the source

of transistor 212 through the drain of transistor 212. From there, the same operation as described above occurs. The current through transistor 213 is decreased from point B to point C as seen in Figure 7H.

[0028] Figure 3 illustrates current Ir supplied by current generator transistor 310 which is controlled by the bias voltage that is generated in current bias generator of current comparator and current bias generator 120 of Figure 1 . Transistor 313 and transistor 314 as seen in Figure 3 correspond to the main differential pair transistors 213 and 214 as seen in Figure 2. Transistor 315 in Figure 3 corresponds to transistor 215 of Figure 2.

[0029] "It" refers to the tail current for the maximum output current of the sinusoidal current waveform. It can be controlled to set the current amplitude of the sinusoidal waveform. Current It of current source 320 in Figure 3 is same current as It as seen in Figure 2. Transistor 313 and transistor 314 share the current It from current source 320 as seen in Figure 3. The current It*a from flows through transistor 313. The current It*a is mirrored by the current mirror generator transistor 311 to transistor 312. The current It*(2*a-1) is subtracted from the mirrored current It*a. Finally, transistor 314 shares part of current It*(1-a). In operation, the gate-source voltages of transistor 313 and transistor 314

are determined. The "a" refers to the distortion control coefficient. The value of "a" is set for the appropriate amplitude of the triangular waveform. If "a" is 99%, the current ratio of transistor 313 to transistor 314 is 99:1, and transistor 314 is slightly ON. The current ratio of transistor 313 and transistor 314 determines the voltage difference between node VH 330 and node VL 331. When "a" is a large ratio that is less than 100%, VH-VL refers to the maximum peak-to-peak voltage of the triangular waveform. When "a" is a small ratio that is more than 0%, VL-VH refers to the maximum peak-to-peak voltage of the triangular waveform. In order to reduce the MOSFETs back-gate effect on transistor 313 and transistor 314, the gate-source voltage of the transistor 315 in Figure 3 must have the same gate-source voltage of transistor 315 in Figure 2. Current Ir from transistor 310 generates the same gate-source voltage of transistor 315 as the gate-source voltage of transistor 315 as seen in Figure 2.

[0030] Figure 4 illustrates the voltage-to-current converter and the switches necessary to rectify the triangular waveform. The transistor 410, transistor 411, transistor 412 and transistor 413 are employed as switches to transmit currents directly or to exchange currents. As seen in Figure 4, the triangular waveform differential voltages are input to

node inp 420 and node inm 421. Also as seen therein, node inp 420 and node inm 421 are connected to gates of transistor 414 and transistor 415. Resistor 430 is coupled to the sources of transistor 414 and transistor 415. The differential input voltage appears as the voltage across resistor 430. Resistor 430 generates a current that is proportional to the differential input voltage. The current flows through the sources through the drains of transistor 414 and transistor 415. As seen in Figure 4, "sw" refers to the input for swapping the polarity of the output currents. When node sw 422 is high transistor 410 and transistor 411 turn off and transistor 412 and transistor 413 turn on. When the input at node sw 422 is low, the current flows in transistors 410, or transistor 411 to node op 423 and node om 424. The terms om and op refer to the current output. When the input at node sw 422 is high, the current flows in transistors 412 or transistor 413, to node om 422 and node op 423.

[0031] Figure 5 illustrates the operation of the voltage-to-current converters. The reference differential voltages are input to node inpgm 520 and node inmgm 521. As seen therein, node inpgm 520 and node inmgm 521 are connected to the gates of transistor 510 and transistor 511. Resistor 530 is coupled to the sources of transistor 510 and transistor 511. The differential input voltage appears as the voltage across resistor 530. Resistor 530

generates a current that is proportional to the input differential reference voltage. The current flows through the source to the drain of transistor 510 and transistor 511, to node opgm 522 and node omgm 523.

[0032] Figure 6 illustrates the current comparator and current bias voltage generator 120 of Figure 1. As seen therein, current is applied at node ip 620 and node im 621. The current input from node ip 620 is mirrored by current mirror generator transistor 610 to transistor 611.

[0033] The mirrored current is also mirrored by current mirror transistor 616 to transistor 617. The current input at node im 621 is mirrored by current mirror transistor 612 to transistor 613. In operation, the current mirrored by transistor 617 subtracts from the current mirrored by transistor 613. The node cmpo 640 is an output of the current comparator that has high output resistance. Node cmpo 640 has a finite output resistance that is determined by the parallel output resistance of transistor 617 and transistor 613. This finite output resistance determines the trans-resistance of this comparator. The trans-conductance of the voltage-to-current converter and this trans-resistance makes a finite gain of the comparator on node cmpo 640. The voltage of the node cmpo 640

generates a reference current with the resistor 630. The current generates the reference bias voltage of the core of the triangular waveform generator.